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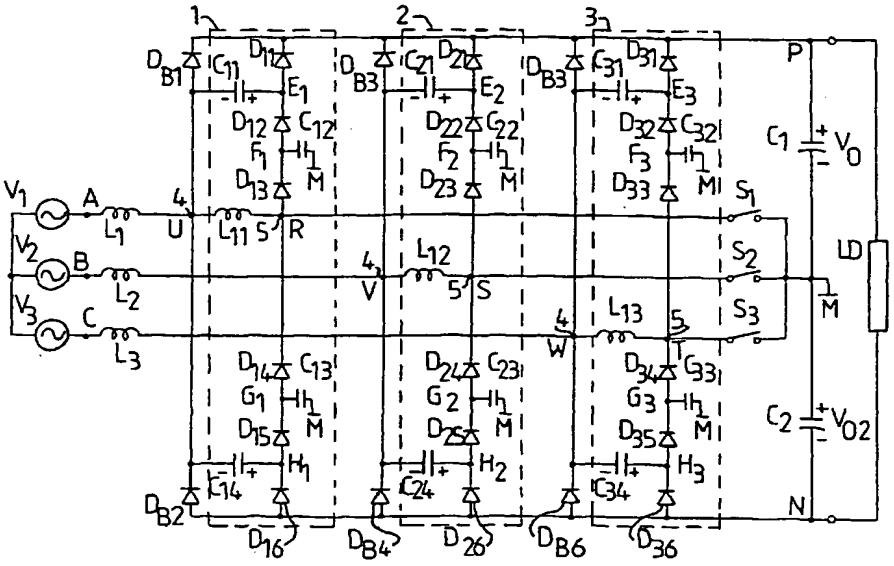
(54) Title: AN ARRANGEMENT FOR AN ELECTRICAL CONVERTER



(57) Abstract: A converter, adapted to be connected to a three-phase input voltage system (V1, V2, V3), comprising a first terminal (P) and a second terminal (N) of a DC voltage output is presented. It comprises for each phase of the input voltage system, two boost diodes (DB1, DB2, DB3, DB4, DB5, DB6), a switch (S1, S2, S3) and a snubber circuit (1, 2, 3). For each phase, a snubber inductor (L11, L12, L13) in series with each switch (1,2,3) reduces the current rising rate at the turn-on instant. When the switch (1,2,3) is turned-off a capacitor (C12, C13, C22, C23, C32, C33) delays the voltage rising by diverting the current that is circulating through the switch. The invention presents a very efficient converter having only one inductor per snubber circuit, which saves both space and cost.

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AN ARRANGEMENT FOR AN ELECTRICAL CONVERTER

TECHNICAL FIELD

The present invention relates to a converter, adapted to be connected to a three-phase input voltage system, according to the preamble of claim 1.

TECHNICAL BACKGROUND

In the use of electronic rectifiers or static converters AC-DC, utility pollution problems may occur caused by large distorted harmonics currents drawn from the power distribution systems. Harmonic currents cause additional harmonic losses in the utility system and may excite electrical resonances, leading to large over-voltages, thus disturbing other sensitive loads connected to the same supply.

Multilevel converters reduce the voltage imposed across the switching devices proportionally with the number of levels. In this way, it is possible to use them in high voltage systems increasing the converter capability. Also, they improve the voltage and current waveforms, which results in a reduction of the harmonic distortion. Additionally, the electromagnetic interference of multilevel converters is smaller than that of conventional converters because the voltage variation (dv/dt) at the commutation instant is divided by the number of levels.

A unidirectional three-phase three-level converter is presented by [K. Oguchi and Y. Machi, "Proposal of a Multilevel-Voltage Source Type Rectifier Having a Three-Phase Diode Bridge Circuit as a Main Power Circuit", Trans. IEEE Japan, Vol. 112D, No. 5, May 1992, pp. 497-498, 1992]. A diode bridge rectifier and three switches with reversible current flow capability compose the converter. The active switches are gated at the same line frequency. The bi-directional switches are gated on at zero crossing of the corresponding phase-voltage. The configura-

tion according to the article in question does not allow output voltage control and the harmonic distortion may increase if the conduction angle of the switches is chosen to be different than 30 degrees. Therefore, the applications for this type of control are limited.

To improve the line-current waveform and the controllability of the three-level converter, pulse width modulation (PWM) is commonly used. The input current is controlled by varying the pulse width of the switching devices, which usually operates at high frequency.

To reduce the energy dissipated in the switching device at the commutation instant, a snubber circuit is required, which limits the current and voltage rising rate at the time of turning on and off, respectively. An advantage of snubber circuits is that they can reduce the EMI (electromagnetic interference) caused by the switching action in the converter.

Constant frequency resonant-transition converters combine resonant methods for low loss switching with PWM for control.

Passive snubbers are preferred to active snubbers because no additional active components are needed, which reduce cost and complexity, and increase robustness and reliability.

Fig. 1 shows a circuit of a passive snubber for a three-level AC-DC converter, introduced in [C. Cruz and I. Barbi, "A passive lossless snubber for the high power factor unidirectional three-phase three-level rectifier", Proceedings of IECON '99, Vol. 2, pp. 909–914, 1999]. The snubber restricts the growth rates of the reverse recovery current and switch voltage with passive components only. The converter has a high efficiency and the snubber is essentially loss-less. However, the snubber requires a relative large number of passive components. This

contributes, not only to a high cost for its production, but also a large footprint in the printed-board, which, in turn, contributes to a large system size and a relatively small power density. The energy due to the turn-on and turn-off process is first stored in an inductive and capacitive element respectively and thereafter is delivered to the load performing the so-called "loss-less" commutation.

SUMMARY

It is an object of the present invention to present a unidirectional three-level converter presenting the advantages of prior art converters and which will have a high power density.

It is another object of the present invention to present a unidirectional three-level converter with a high efficiency and low electromagnetic interference.

The objects are met with a converter, adapted to be connected to a three-phase input voltage system, having the characterizing features of claim 1.

The snubber inductor in series with each switching device reduces, during operation, the current rising rate at the turn-on instant of the switch, so that turn-on commutations are performed with initially zero and then slow rising current. It is connected between the junction of two boost diodes and a bi-directional switch, and prevents the dangerous effect that the boost-diode recovery currents have on the switches.

According to the invention only one inductor is used to prevent the reverse recovery current of both boost diodes in each phase. Thus, the same inductor is used in both the positive and in the negative semi cycle of the input voltage, and the invention allows the saving of one resonant inductor per phase. Therefore,

compared with the state of the art, the circuit related with the present invention allows the savings of three resonant inductors.

The resonant inductors are among the most volume intensive components, and obviously are also among the most expensive elements of the circuit. Therefore, reducing the number of resonant inductors will reduce the cost and the volume of the complete system, and increase the power density.

Preferably the means to limit a voltage rise comprises a second and a third snubber capacitor. When the switching device is turned-off these capacitors will delay the voltage rise by diverting the current that is circulating through the switch.

The "loss-less snubbing" is performed by storing the energy due to the switching process in passive elements (inductors and capacitors) and thereafter transferring the energy to a load.

It is important to remark that the invention keeps the advantageous characteristics of the three-level boost-type converters such as: low voltage stress on the switching devices, high quality waveforms, no shot-though possibility and generation of two symmetrical output voltages. The converter according to the invention operates with soft commutation without the employment of auxiliary switches.

BRIEF DESCRIPTION OF THE FIGURES

The invention will now be described in greater detail with reference to the drawing, in which

- fig. 1 shows a three-phase three-level converter with a passive snubber according to prior art,

- fig. 2 shows a simplified circuit diagram of a three-phase, three-level boost-type converter with a passive snubber according to a preferred embodiment of the invention,
- fig. 3a-3f show alternative details of the converter in fig. 2,
- fig. 4 shows diagrams of voltage and current in the circuit in fig. 2,
- fig. 5 shows a printed board layout of a converter according to prior art,
- fig. 6 shows a printed board layout of a converter according to the invention,
- fig. 7 shows a simplified circuit diagram of a three-phase, three-level boost-type converter with a passive snubber according to an alternative embodiment of the invention, and
- fig. 8 shows a simplified circuit diagram of a three-phase, three-level boost-type converter with a passive snubber according to another embodiment of the invention.

DETAILED DESCRIPTION

Fig. 2 shows the circuit design of the three-level converter according to a preferred embodiment of the invention. The converter is connected to a three-phase voltage system V1, V2, V3 through three boost inductors L1, L2, L3. One out of two terminals in each boost inductor L1, L2, L3 is connected to a point A, B, C, respectively. The other terminal of each boost inductors is connected to a point U, V and W, respectively.

The converter comprises first DB1, DB3, DB5 and second DB2, DB4, DB6 boost diodes. The anodes of the first boost diodes DB1, DB3, DB5 and the cathodes of the second boost diodes second DB2, DB4, DB6 are connected to points U, V and W, respectively. The cathodes of the first boost diodes DB1, DB3, DB5 are connected to a point P, which represents the positive terminal of a DC voltage output. Similarly, the anodes of the second boost diodes DB2, DB4, DB6 are

connected to a point N representing the negative terminal of the voltage output. The points P and N are adapted to have a load LD connected between them.

There are two capacitors connected at the output terminals. A first output capacitor C1 is connected between the positive terminal P and a medium point M, which is a reference for the positive and negative output voltages at points P and N, respectively. A second output capacitor C2 is connected between the medium point M and the negative terminal N.

Three bi-directional switches S1, S2 and S3 are connected to the medium point M in one end, and to points R, S and T, respectively, at another end. The bi-directional switches are represented as ideal switches in Fig. 2. In practice they may have any of the configurations shown in Fig. 3a-3f.

There are three passive snubber circuits 1, 2, 3 connected between the boost diodes and the bi-directional switches. (In fig. 2 each snubber circuit 1, 2, 3 is indicated as enclosed by a rectangle of broken lines.) The snubber circuits have similar configuration and each of them comprises a first C11, C21, C31, a second C12, C22, C32, a third C13, C23, C33 and a fourth C14, C24, C34 snubber capacitor, as well as a first D11, D21, D31 a second D12, D22, D32, a third D13, D23, D33, a fourth D14, D24, D34, a fifth D15, D25, D35 and a sixth snubber diode D16, D26, D36. Preferably the snubber diodes are of an ultra fast type. Additionally, each snubber circuit 1, 2, 3 comprises a snubber inductor L11, L12. L13.

The snubber circuit 1 is connected to the rectifier as follows. The snubber inductor L11 is, at a first snubber inductor terminal 4, connected to a point U, which is a junction of the first and the second boost diodes DB1, DB2, and, at a second snubber inductor terminal 5, connected to the bi-directional switch S1 via a point R.

The snubber inductor L11 reduces the slope rate of the current through the switch S1 at a turn-on instant thereof. This avoids the dangerous effect that the boost-diode recovery currents have on the switches. According to the invention, for each phase only one inductor is used to prevent the reverse recovery current of both diodes.

The third and fourth snubber diode D13, D14 join the snubber inductor L11 with the second and third snubber capacitor C12, C13, respectively, and prevent discharge of the second and third snubber capacitor C12, C13 through the switch S1 at a turn-on instant of the switch. The anode of the third snubber diode D13 is connected to the point R and the cathode thereof to a point F1. The cathode of the fourth snubber diode D14 is connected to the point R and the anode thereof to a point G1.

The second and third capacitors C12, C13 are used to limit the voltage rise on S1 at the turn-off instant of the switch. They are, in one end, connected together at the point M. The other end of the second snubber capacitor C12 is connected to the point F1 and the other end of the third snubber capacitor C13 is connected to the point G1.

The second snubber diode D12 creates a path to transfer the energy due to the commutations from the snubber inductor L11 and the second snubber capacitor C12 to the first snubber capacitor C11. Similarly, the fifth snubber diode D15 creates a path to transfer the energy due to the commutations from the snubber inductor L11 and the third snubber capacitor C13 to the fourth snubber capacitor C14. This energy is thereafter transferred to the load LD to avoid commutation losses. The anode of the second snubber diode D12 is connected to the point F1 and the cathode thereof to a point E1. The anode of the fifth snubber diode D15 is connected to a point H1 and the cathode thereof to the point G1.

The first and fourth snubber capacitors C11, C14 temporally store the commutation energy, which is thereafter transferred to the load LD via the first and sixth snubber diodes, D11 and D16, respectively. The first and fourth snubber capacitors C11 and C14 are connected together at one end to the point U and at the other end to the points E1 and H1, respectively.

Finally, the diodes D11 and D16 create the necessary path to transfer the energy stored in C11 and C14 to the load LD. The anode of the first snubber diode D11 is connected to the point E1 and cathode thereof to the positive output terminal P. The cathode of the sixth snubber diode D16 is connected to the point H1 and anode thereof to the negative output terminal N.

The snubbers 2 and 3 are connected to the rectifier in the same manner as the snubber 1, described above.

Fig. 4 shows, as functions of time, the currents through the snubber inductor L11, i(L11), and the switch S1, i(S1), and the voltage across the switch S1, v(S1), the second snubber capacitor C12, v(C12), and the first snubber capacitor C11, v(C11). To make understanding easier it is assumed that the current that flows through the boost inductor L1, here referred to as input current, is constant at a value I, during the switching period. Similarly, the voltage across the first output capacitor C1, here referred to as output voltage, remains constant at a value Vo1.

Initially, before t0, the switch S1 is in blocking condition and the input current flows through the boost inductor L1 and the first boost diode DB1 to the first output capacitor C1 and the load LD. The current through the snubber inductor L11, i(L11), and the switch S1, i(S1), is equal zero, while the voltage across the second snubber capacitor C12, v(C12), and the switch S1, v(S1), is equal to Vo1 and the voltage across the first snubber capacitor C11, v(C11), is equal to zero.

At the time t0 the switch S1 is turned to conduction condition and since the first boost diode DB1 is also in conducting state, the output voltage Vo1 is applied across the terminals 4, 5 of the snubber inductor L11. Therefore, the current through the snubber inductor L11, i(L11), and switch S1, i(S1), will increase with a rate given by:

$$\frac{di}{dt} = \frac{Vo1}{L11}$$

The current circulating through the first boost diode DB1 will decrease with the same rate. When this current has dropped to zero it will change direction and continue circulating through the first boost diode DB1 during a small time given by the reverse recovery characteristic of the diode. Thereafter, at a time t1, the first boost diode DB1 will change to blocking state. Until this time voltages across the first snubber capacitor C11, v(C11), and the second snubber capacitor C12, v(C12), remain at zero and Vo1, respectively.

When the first boost diode DB1 turns to blocking condition at the time t1, the second snubber diode D12 will start conducting the current though a loop formed by the second snubber diode D12, the first snubber capacitor C11, the snubber inductor L11, the switch S1 and the second snubber capacitor C12. During a time interval from t1 to t2, the energy stored in the second snubber capacitor C12 is transferred to the first snubber capacitor C11. The voltage across the second snubber capacitor C12 decreases from Vo1 to zero, while the current through the snubber inductor L11 and the switch S1 continues to rise. The resonant transition from t1 to t2 is governed by the equation for the current through the snubber inductor L11, i(L11), given by

$$i_{L11}(t) = I + \frac{Vo1}{\omega \cdot L11} \cdot \sin(\omega \cdot t)$$

and the voltage across the second snubber capacitor C12, v(C12), given by

$$v_{C12}(t) = Vo1 \cdot \frac{\omega 2^2}{\omega^2} \cdot \left[\cos(\omega t) + \frac{\omega^2}{\omega 2^2} - 1 \right].$$

The voltage across the first snubber capacitor C11, v(C11) is given by

$$v_{C11}(t) = Vo1 \cdot \frac{\omega 1^2}{\omega^2} \cdot [1 - \cos(\omega t)]$$

where

$$\omega = \frac{1}{\sqrt{L11 \cdot C}},\ C = \frac{C11 \cdot C12}{C11 + C12},\ \omega 1 = \frac{1}{\sqrt{L11 \cdot C11}} \text{ and } \omega 2 = \frac{1}{\sqrt{L11 \cdot C12}}.$$

Once the second snubber capacitor C12 is totally discharged at the time t2, the third snubber diode D13 turns to conducting state, and the inductor current starts to circulate in a loop formed by the diodes D13, and D12, the first snubber capacitor C11 and the snubber inductor L11. The current through the switch S1 is no longer equal to the current through the snubber inductor L11. While the switch S1 carries the input current I to the load LD, the snubber inductor L11 carriers the input current I plus the current that circulates through the loop formed by D13, D12, the first snubber capacitor C11 and the snubber inductor L11. During a time interval from t2 to t3, the energy stored in the snubber inductor L11 is transferred to the first snubber capacitor C11. During this stage the current through the snubber inductor L11 decreases, until it equalizes the input current I at the time t3. During the resonant stage from t2 to t3 the current through the snubber inductor L11, i(L11), is given by

$$i_{L11}(t) = I + \frac{Vo1 \cdot \sqrt{2 \cdot \omega 2^2 - \omega^2}}{\omega 2^2 \cdot L11} \cdot \cos(\omega 1 \cdot t) - \frac{Vo1 \cdot \omega 1}{\omega 2^2 \cdot L11} \cdot \sin(\omega 1 \cdot t)$$

and the voltage across the first snubber capacitor C11, v(C11), is given by

$$v_{C11}(t) = \frac{Vo1 \cdot \omega 1^2}{\omega 2^2} \cdot \cos(\omega 1 \cdot t) + \frac{Vo1 \cdot \omega 1 \cdot \sqrt{2 \cdot \omega 2^2 - \omega^2}}{\omega 2^2} \cdot \sin(\omega 1 \cdot t)$$

Once the current through the snubber inductor L11 equalizes to the input current at t3, the currents and voltages in the resonant elements (the snubber inductor L11, the first snubber capacitor C11 and the second snubber capacitor C12) and the switch S1 remain constant. This stage ends at t4 when the switch S1 is turned to blocking condition. Preferably the switch is controlled by a gate command signal.

At the time t4, the input current that was circulating through the switch S1 is deviated to the second snubber capacitor C12 via the third snubber diode D13. The voltage across the second snubber capacitor C12, v(C12), that was zero at t4, increases linearly with a rate given by

$$\frac{dv}{dt} = \frac{I}{C12}$$

This stage ends at t5 when the sum of voltage across the first snubber capacitor C11 plus voltage across the second snubber capacitor C12 equals to the output voltage Vo1. The current through the snubber inductor L11 and the voltage across the first snubber capacitor C11 remain constant during this interval from t4 to t5.

At the time t5 the first snubber diode D11 is directly polarized and starts to carry part of the input current toward the output. The residual part of the input current

remains circulating through the second snubber capacitor C12, which continues charging until the voltage across its terminals equals Vo1. During the resonant stage at the time interval from t5 to t6, the current through the snubber inductor L11 is

$$i_{L11}(t) = I - \frac{I \cdot C}{C12} \cdot [1 - \cos(\omega \cdot t)]$$

and the voltage across the first snubber capacitor C11 is

$$v_{C11}(t) = \frac{I \cdot C}{C11 \cdot C12 \cdot \omega} \cdot \sin(\omega \cdot t) - \frac{I \cdot C}{C11 \cdot C12} \cdot t + Vo1 \cdot \frac{\omega 1}{\omega 2}$$

and the voltage across the second snubber capacitor C12 is

$$v_{C12}(t) = \frac{I \cdot C}{C12^2 \cdot \omega} \cdot \sin(\omega \cdot t) + \frac{I}{C11 \cdot C12} \cdot t + Vo1 - Vo1 \cdot \frac{\omega 1}{\omega 2}$$

When the voltage across the second snubber capacitor C12 equalizes Vo1 at the time t6, the second snubber diode D12 becomes directly polarized and starts to conduct part of the input current toward the load LD via the first snubber diode D11. The remainder of the input current continues to circulate through the first snubber capacitor C11 and the first snubber diode D11. The current through the snubber inductor L11 continues falling until the time t7, at which it reaches zero. Since the time interval between t5 and t6 is very small, to obtain the equations valid for this resonant stage, it has been considered that the values of current and voltages at t6 are the same as those values at t5. With this simplification the equations valid in the time interval from t6 to t7 are the following:

For the current through the snubber inductor L11:

$$I_{l11}(t) = I - \frac{Vo1}{L11 \cdot \omega 2} \cdot \sin(\omega 1 \cdot t)$$

For the voltage across the first snubber capacitor C11:

$$v_{C11}(t) = Vo1 \cdot \frac{\omega 1}{\omega 2} \cdot \cos(\omega 1 \cdot t)$$

The voltage across second snubber capacitor C12 remains unchanged at Vo1.

At the time t7, the current through the snubber inductor L11 becomes zero and remains at this value. During the time interval from t7 to t8, the input current circulates through the first snubber capacitor C11 and the first snubber diode D11 to the load LD. The voltage across the first snubber capacitor C11 is reduced with a constant rate until it reaches zero value. The equation that determines the voltage across the first snubber capacitor C11 is:

$$v_{C11}(t) = \frac{\omega 1}{\omega 2} \cdot \sqrt{Vo1^2 - I^2 \cdot L11^2 \cdot \omega 2^2} - \frac{I}{C11} \cdot t$$

At the time t8, the voltage across the first snubber capacitor C11 becomes zero and the first boost diode DB1 becomes directly polarized conducting the input current towards the output. Thereafter, the currents and voltages across the snubber elements remain constant until a new cycle is initiated.

The stages described above are valid for the positive semi cycle of the input voltage (phase A) and current commutation from the first boost diode DB1 to the switch S1 and vice-versa. During the negative semi cycle the current commutation occurs from the second boost diode DB2 to the switch S1 with the same corresponding stages. For the negative semi cycle, the elements involved with soft commutations are the snubber inductor L11, the third snubber capacitor C13, the fourth snubber capacitor C14, the fourth D14, the fifth D15 and the sixth D16 snubber diode. It is important to notice that the snubber inductor L11 is used in

the positive and in the negative semi cycle. Thus, the proposed invention allows to save one resonant inductor per phase.

To verify the space savings accomplished by the invention, two compact printed board lay outs have been performed. Fig. 5 shows the printed board layout of the converter proposed by Cruz et al, and depicted in fig. 1. Fig. 6 shows the printed board layout of the converter according to the invention. As can be seen, the circuit according to the invention can be placed in a smaller printed board area, which saves cost and reduces the total size of the converter.

Since the electrical stress placed on the devices during switching is reduced, it is possible to increase the switching frequency of the converter and therefore, improve the waveforms generated. Any PWM control method for the three-phase three-level boost type converter could be used to control the input currents and output voltages. Such a control method is described in [R. Rojas, "Método e Circuito de Controle Para Retificador do Tipo Elevador Trifásico de Três Níveis" – patent PI 9907351-0].

Fig. 7 shows a circuit diagram of a converter according to an alternative embodiment of the invention. As can be seen in fig. 7, in principal this circuit is similar to the circuit in fig. 2. However, in each snubber circuit the anode of the second snubber diode D12, D22, D32 is connected directly to the second snubber inductor terminal 5, and the anode of the fourth snubber diode D14, D24, D34 is connected directly to the fourth snubber capacitor C14, C24, C34 and the cathode of the sixth snubber diode D16, D26, D36. The absence of the second C12, C22, C32 and third C13, C23, C33 snubber capacitors and the third D13, D23, D33 and the fifth D15, D25, D35 snubber diodes will result in a snubber circuit that will only limit the losses at turn-on instant, i.e. reduce the current increase at turn-on instant. The losses due to the turn-off of the switch will not be reduced in this case.

Fig. 8 shows a simplified circuit diagram of a three-phase, three-level boost-type converter with a passive snubber according to another embodiment of the invention. The converter is connected to two loads LD1, LD2, one LD1 between the first terminal P and the medium point M, and the other LD2 between the second terminal N and the medium point. The loads LD1, LD2 should be essentially symmetrical, but the arrangement allows for a small asymmetry in the loads.

CLAIMS

1. A converter, adapted to be connected to a three-phase input voltage system (V1, V2, V3), comprising a first terminal (P) and a second terminal (N) of a DC voltage output, adapted to be connected to at least one load (LD), a medium point (M), adapted to provide a reference for a positive and negative voltage of the DC voltage output, and, for each phase of the input voltage system,
   - a first boost diode (DB1, DB3, DB5) and a second boost diode (DB2, DB4, DB6) the cathodes of which are connected to the first terminal (P) of the DC voltage output and the respective phase of the input voltage system (V1, V2, V3), respectively, and, the anodes of which are connected to the respective phase of the input voltage system (V1, V2, V3) and the second terminal (N) of the DC voltage output, respectively,
   - a switch (S1, S2, S3) connected to the medium point (M) and adapted to undergo a switching process,
   - a snubber circuit (1, 2, 3) connected to the first terminal (P) and the second terminal (N) and comprising means to store and transfer to the load (LD) energy caused by the switching process,

   characterized in that the means to store and transfer to the load (LD) energy caused by the switching process comprises a snubber inductor (L11, L12, L13), at a first snubber inductor terminal (4), connected to the respective phase of the input voltage system (V1, V2, V3) and, at a second snubber inductor terminal (5), connected to the switch (S1, S2, S3).

2. A converter according to claim 1, at which each snubber circuit (1, 2, 3) further comprises a first snubber diode (D11, D21, D31), a second snubber diode (D12, D22, D32), a fourth snubber diode (D14, D24, D34), a sixth snubber diode (D16, D26, D36), a first snubber capacitor (C11, C21, C31), and a fourth snubber capacitor (C14, C24, C34), at which

- the cathode of the second snubber diode (D12, D22, D32) is connected to the anode of the first snubber diode (D11, D21, D31) and the anode of the second snubber diode (D12, D22, D32) is connected to the second snubber inductor terminal (5),
- the first snubber capacitor (C11, C21, C31) is connected between the first snubber inductor terminal (4) on one side, and the anode of the first snubber diode (D11, D21, D31) and the cathode of the second snubber diode (D12, D22, D32) on the other side,
- the cathode of the first snubber diode (D11, D21, D31) is connected to the first terminal (P) of the DC voltage output,
- the cathode of the fourth snubber diode (D14, D24, D34) is connected to the second snubber inductor terminal (5),
- the fourth snubber capacitor (C14, C24, C34) is connected between the first snubber inductor terminal (4) on one side, and the anode of the fourth snubber diode (D14, D24, D34) and the cathode of the sixth snubber diode (D16, D26, D36) on the other side, and
- the anode of the sixth snubber diode (D16, D26, D36) is connected to the second terminal (N) of the DC voltage output.

3. A converter according to claim 2, at which the means to store and transfer to the load (LD) energy caused by the switching process comprises a second (C12, C22, C32) and a third snubber capacitor (C13, C23, C33), and each snubber circuit further comprises a third snubber diode (D13, D23, D33), a fifth snubber diode (D15, D25, D35), at which
- the anode of the third snubber diode (D13, D23, D33) is connected to the second snubber inductor terminal (5),
- the second snubber capacitor (C12, C22, C32) is connected between the medium point (M) on one side and the cathode of the third snubber diode (D13, D23, D33) and the anode of the second snubber diode (D12, D22, D32) on the other side,

- the third snubber capacitor (C13, C23, C33) is connected between the medium point (M) on one side and anode of the fourth snubber diode (D14, D24, D34) and the cathode of the fifth snubber diode (D15, D25, D35) on the other side, and
- the anode of the fifth snubber diode (D15, D25, D35) is connected to the cathode of the sixth snubber diode (D16, D26, D36) and the fourth snubber capacitor (C14, C24, C34).

4. A converter according to claim 1, 2 or 3, at which a boost inductor (L1, L2, L3) is connected between each phase of the input voltage system, and the anode of the respective first boost diode (DB1, DB3, DB5), the cathode of the respective second boost diode (DB2, DB4, DB6) and the first snubber inductor terminal of the first snubber inductor (L11, L12, L13).

5. A converter according to claim 1, 2, 3 or 4, at which a first output capacitor (C1) is connected between the first terminal (P) and the medium point (M), and a second output capacitor (C2) is connected between the second terminal (N) and the medium point (M).

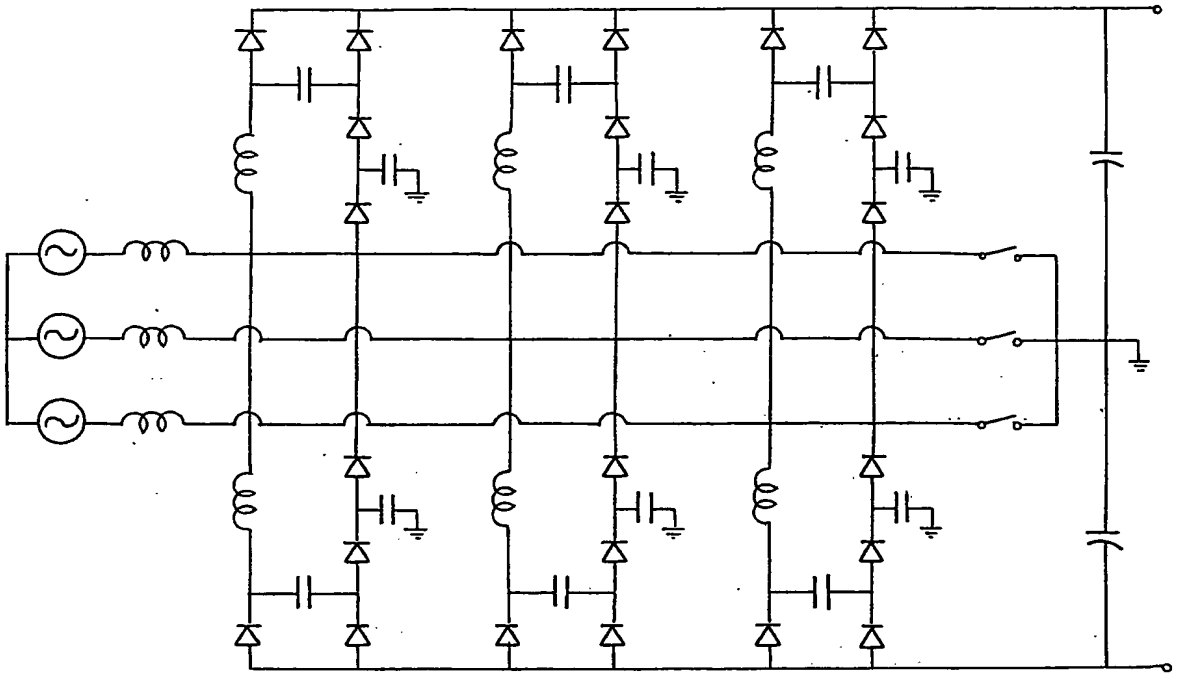

FIG.1

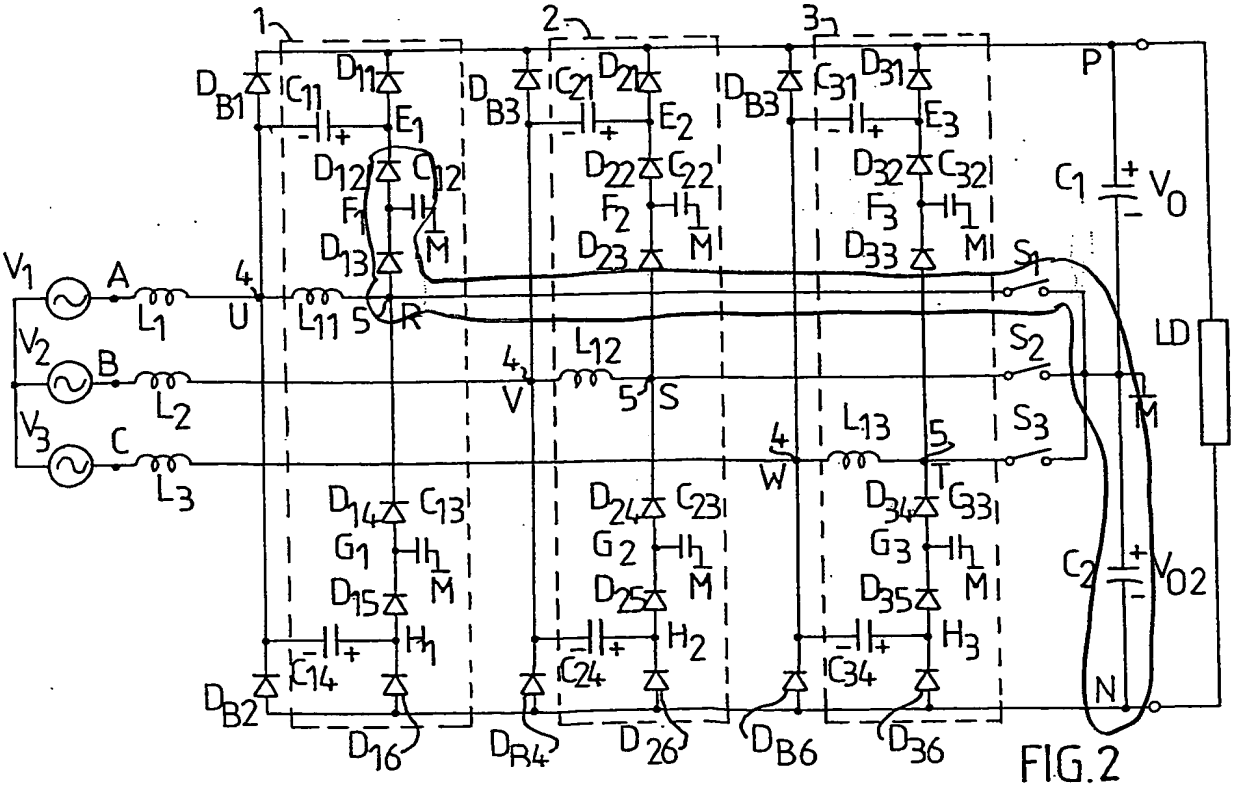
1
2
3
P
N
LD
A
B
C
U
V
W
R
S
M
L1
L2
L3
L11
L12
L13
S1
S2
S3
C1
V0
C2
V02
V1
V2
V3
DB1
DB2
DB3
DB4
DB6
D11
D12
D13
D14
D15
D16
D21
D22
D23
D24
D25
D26
D31
D32
D33
D34
D35
D36
C11
C12
C13
C14
C21
C22
C23
C24
C31
C32
C33
C34
E1
E2
E3
F1
F2
F3
G1
G2
G3
H1
H2
H3

FIG.2

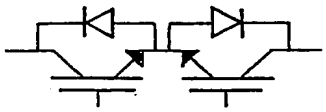

FIG.3a

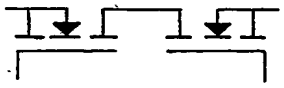

FIG.3b

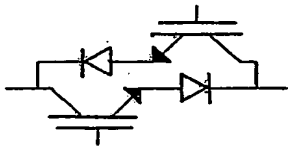

FIG.3c

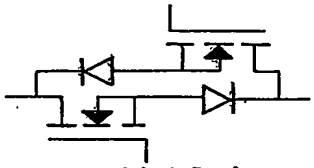

FIG.3d

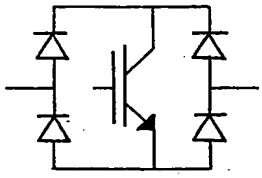

FIG.3e

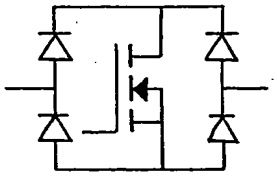

FIG.3f

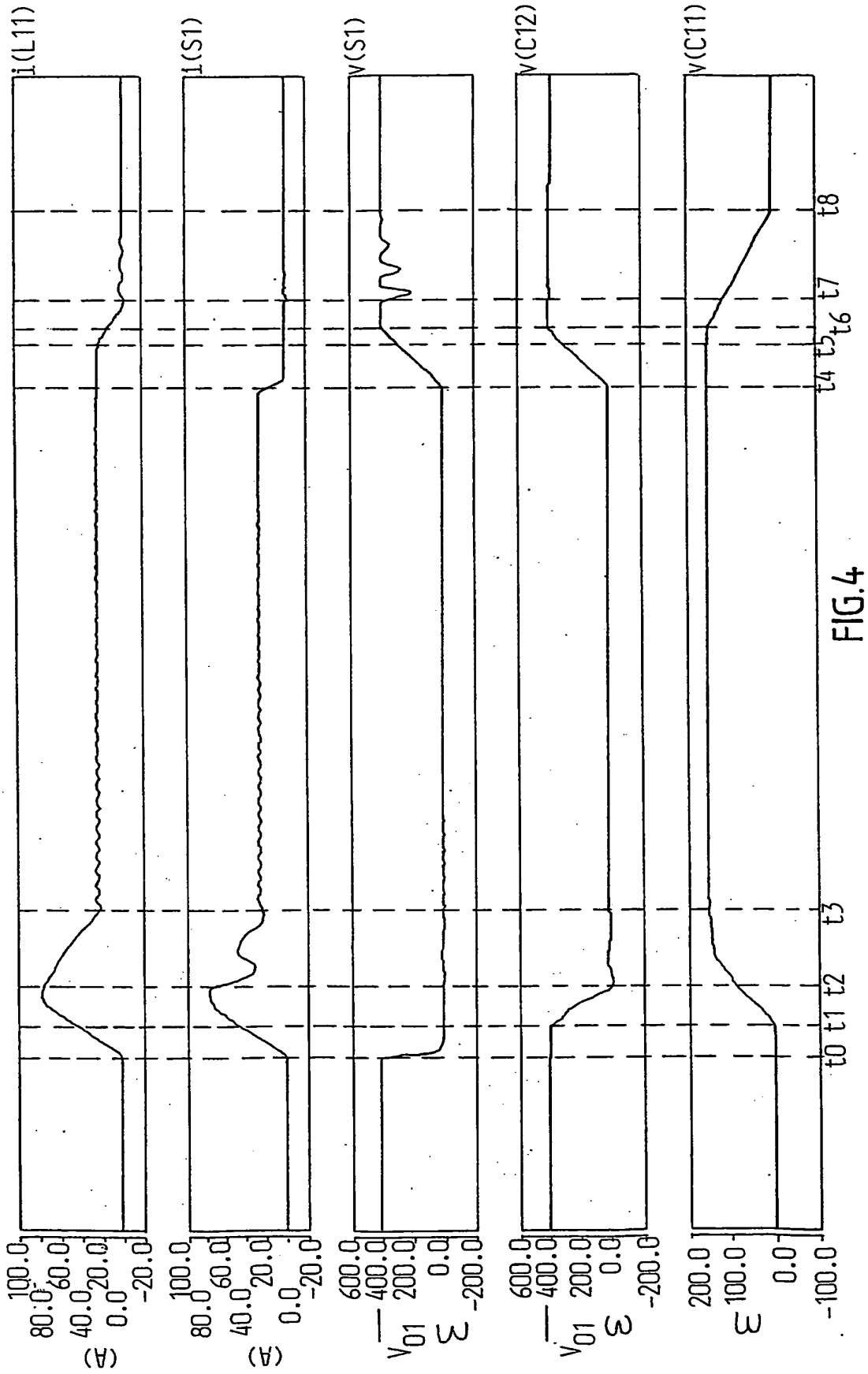
i(L11)
i(S1)
v(S1)
v(C12)
v(C11)
t0 t1 t2 t3 t4 t5 t6 t7 t8
100.0
80.0
60.0
40.0
20.0
0.0
-20.0
(A)
600.0
400.0
200.0
0.0
-200.0
ω_{01}
200.0
100.0
0.0
-100.0
ω

FIG.4

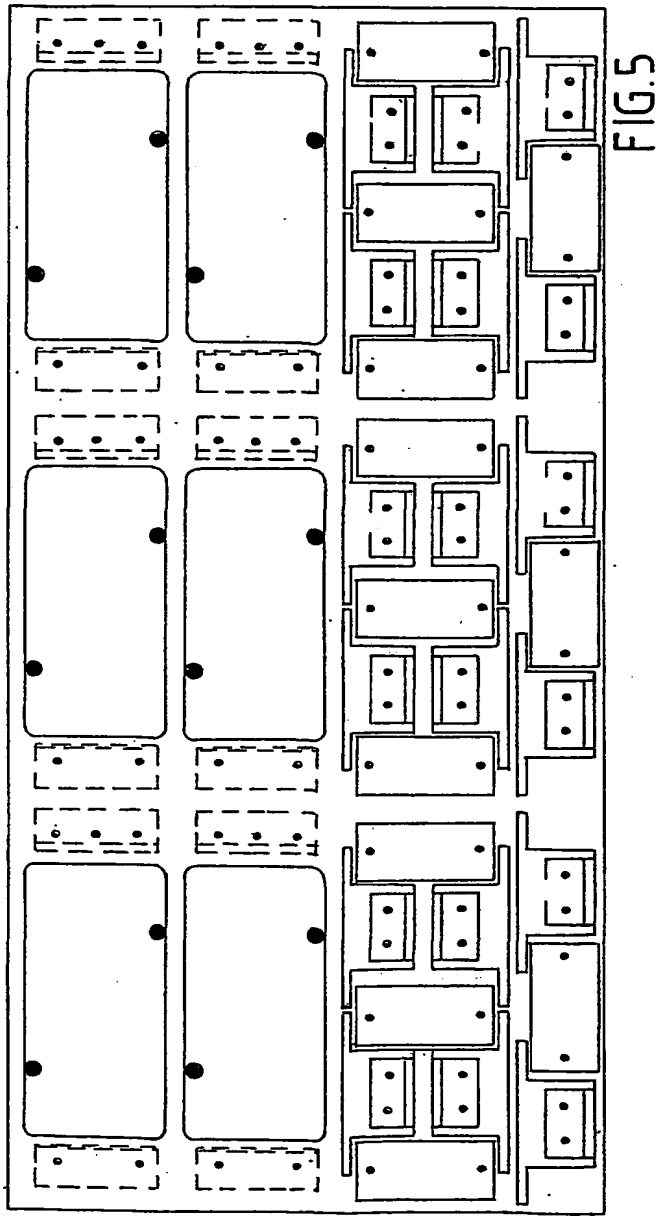

FIG.5

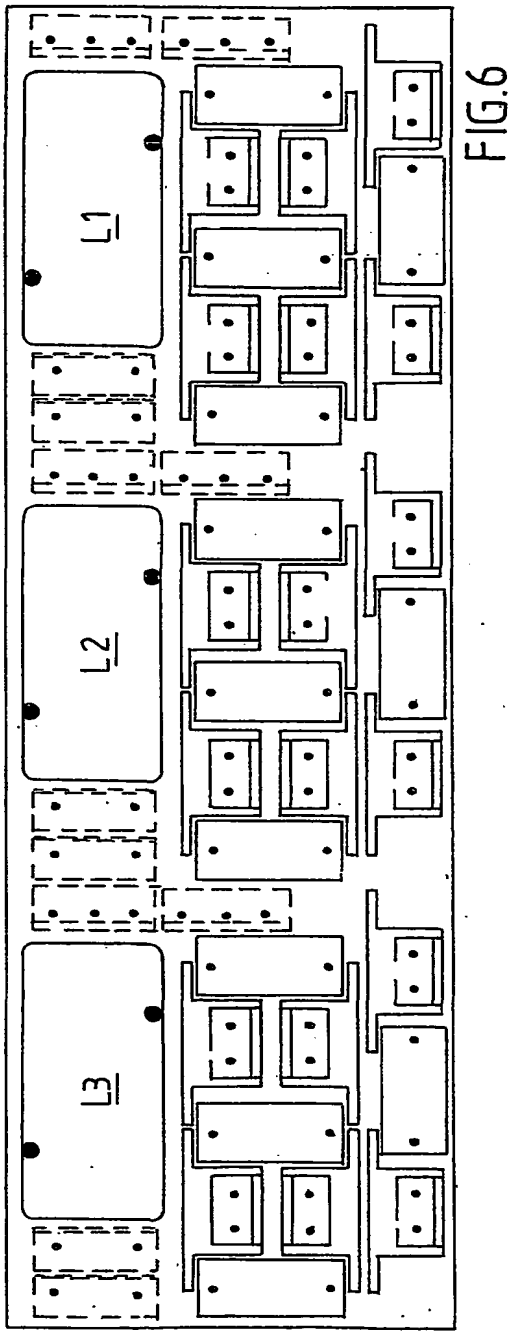

FIG.6

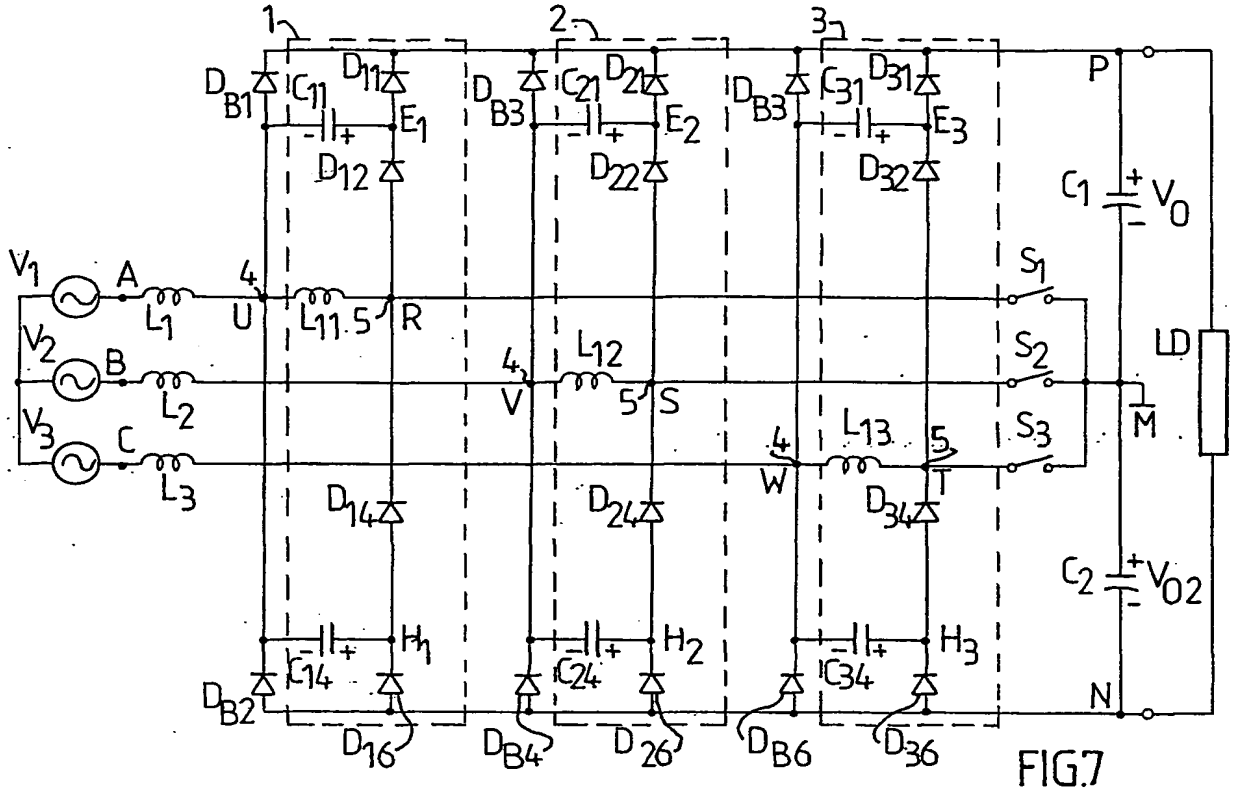
1
2
3
P
N
M
A
B
C
U
V
W
R
S
T
LD
V_1
V_2
V_3
L_1
L_2
L_3
L_{11}
L_{12}
L_{13}
C_1
V_0
C_2
V_{02}
S_1
S_2
S_3
D_{B1}
D_{B2}
D_{B3}
D_{B4}
D_{B6}
C_{11}
C_{21}
C_{31}
E_1
E_2
E_3
D_{11}
D_{21}
D_{31}
D_{12}
D_{22}
D_{32}
D_{14}
D_{24}
D_{34}
H_1
H_2
H_3
C_{14}
C_{24}
C_{34}
D_{16}
D_{26}
D_{36}

FIG.7

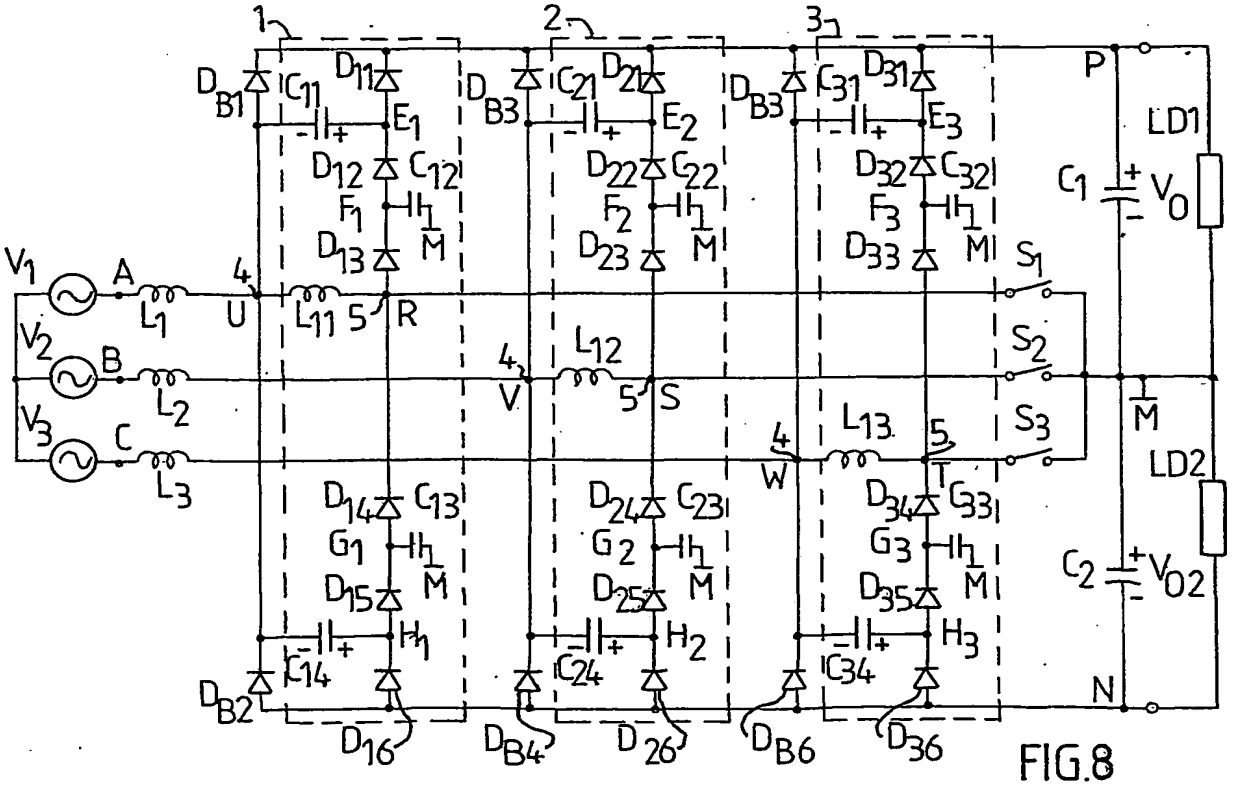
1
2
3
P
N
M
A
B
C
U
V
W
R
S
T
LD1
LD2
V_1
V_2
V_3
L_1
L_2
L_3
L_{11}
L_{12}
L_{13}
C_1
V_0
C_2
V_{02}
S_1
S_2
S_3
D_{B1}
D_{B2}
D_{B3}
D_{B4}
D_{B6}
C_{11}
C_{21}
C_{31}
E_1
E_2
E_3
D_{11}
D_{21}
D_{31}
D_{12}
C_{12}
F_1
D_{13}
D_{22}
C_{22}
F_2
D_{23}
D_{32}
C_{32}
F_3
D_{33}
D_{14}
C_{13}
G_1
D_{15}
D_{24}
C_{23}
G_2
D_{25}
D_{34}
C_{33}
G_3
D_{35}
H_1
H_2
H_3
C_{14}
C_{24}
C_{34}
D_{16}
D_{26}
D_{36}

FIG.8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/01469

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H02M 7/06, H02M 1/12
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Industrial Electronics Society, 1999. IECON '99 Proceedings. The 25th Annual Conference. Vol. 2, 1999, "A passive lossless snubber for the high power factor unidirectional three-phase three-leve rectifier", sid 909 - sid 914 ---	1-5
A	PATENT ABSTRACTS OF JAPAN Vol. 018, no. 286 (E-1556s) 31 May 1994 (1994-05-31) & JP 06 054539 A (OGUCHI KUNIOMI) 25 February 1994 (1994-02-25)2 abstract ---	1-5

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 November 2002	19-11-2002
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Irma Bornhede/MN Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/01469

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN Vol. 2000, no. 15 06 April 2001 (2001-04-06) & JP 2000 358372 A (OGUSHI KUNIOMI ET AL) 26 December 2000 (2000-12-26) abstract -- --------	1-5